

## Lesson Plan

**Name of the Faculty** : **DR. RASHMI DAHRA (PROFESSOR)**  
**Discipline** : **BCA**  
**Semester** : **3rd**  
**Subject** : **Computer System Architecture (BCA-203 B)**  
**Lesson Plan Duration** : **15 weeks (from July, 2018 to Dec., 2018)**

**Work Load (Lecture/Practical) per week (in hours):Lecture: 3, Practical:NA**

Week	Theory		Practical	
	Lecture Day	Topic(including Assignment/Test)	Practical Day	Topic
1st	1 <sup>st</sup>	Introduction to Computer and CPU(Computer Organization, Computer Design and Computer Architecture		
	2 <sup>nd</sup>	Stored ProgramConcept-Von Neumann Architecture.		
	3 <sup>rd</sup>	Introduction to Flynn"s Classification SISD, SIMD,MIMD		
	T1	Tutorial---review of lectures		
2nd	4 <sup>th</sup>	Register Transfer and Micro operations- Introduction to Registers, Register Transfer Language, Data movement among Registers and Memory,		
	5 <sup>th</sup>	Micro operations: Introduction to micro operations, Types of micro operations--Logic Operations,		
	6 <sup>th</sup>	Shift operations, Arithmetic and Shift operations		
	T2	Tutorial---problem/review		

		of lectures		
3rd	7 <sup>th</sup>	Common Bus System : Introduction to Common Bus System		
	8 <sup>th</sup>	Types of Buses(Data Bus, Control Bus, Address Bus),		
	9 <sup>th</sup>	16 bit Common Bus System--Data Movement among registers using Bus.		
	T3	Tutorial---problem/ review of lectures		
4th	10 <sup>th</sup>	Basic Computer Instructions- Introduction to Instruction,		
	11 <sup>th</sup>	Types of Instructions (Memory Reference,)		
	12 <sup>th</sup>	I/O Reference and Register Reference		
	T4	Tutorial---problem/review of lectures		
5th	13 <sup>th</sup>	Instruction Cycle		
	14 <sup>th</sup>	Instruction Formats (Direct and Indirect Address Instructions, Zero Address, One Address, Two Address and Three Address Instructions)		
	15 <sup>th</sup>	Interrupt: Introduction to Interrupt and Interrupt Cycle		
	T5	Tutorial---problem/review of lectures		
6th	16 <sup>th</sup>	Design of Control Unit: Introduction to Control Unit, Types of Control Unit (Hardwired & Micro programmed Control Unit).		
	17 <sup>th</sup>	Addressing Modes- Introduction & different types of Addressing Modes.		
	18 <sup>th</sup>	Assignment on above topics/ Test 3		

7th	19 <sup>th</sup>	I/O Organization: I/O Interface Unit, types of ports (I/O port, Network Port, USB port, Serial and Parallel Port),		
	20 <sup>th</sup>	Concept of I/O bus, Isolated I/O versus Memory Mapped I/O.		
	21 <sup>st</sup>	I/O Data Transfer Techniques: Programmed I/O,		
	T6	Tutorial---problem/review of lectures		
8th	22 <sup>nd</sup>	Interrupt Initiated I/O,		
	23 <sup>rd</sup>	DMA Controller		
	24 <sup>th</sup>	Assignment on above topics/ Test 4		
	T7	Tutorial---problem/review of lectures		
9th	25 <sup>th</sup>	IOP.		
	26 <sup>th</sup>	Synchronous and Asynchronous Data Transfer		
	27 <sup>th</sup>	Concept of strobe and handshaking		
	T8	Tutorial---problem/review of lectures		
10th	28 <sup>th</sup>	source and destination initiated data transfer		
	29 <sup>th</sup>	Stack Organization: Memory Stack and Register Stack		
	30 <sup>th</sup>	Assignment on above topics/ Test5		
	T9	Tutorial---problem/review of lectures		
11th	31 <sup>st</sup>	Memory organization: Memory Hierarchy,		
	32 <sup>nd</sup>	Main Memory (RAM and ROM chips		
	33 <sup>rd</sup>	Logical and Physical Addresses		
	T10	Tutorial---problem/review of lectures		

12th	34 <sup>th</sup>	Memory Address Map, Memory Connection to CPU		
	35 <sup>th</sup>	Associative Memory		
	36 <sup>th</sup>	Cache Memory		
	T11	Tutorial---problem/review of lectures		
13th	37 <sup>th</sup>	Cache Memory (Initialization of Cache Memory, Writing data into Cache, Locality of Reference, Hit Ratio),		
	38 <sup>th</sup>	Replacement Algorithms (LRU and FIFO		
	39 <sup>th</sup>	Assignment on above topics/ Test6		
	T12	Tutorial---problem/ review of lectures		
14th	40 <sup>th</sup>	Cache Memory Mapping Techniques: Direct Mapping,		
	41 <sup>st</sup>	Associative Mapping and SetAssociative		
	42 <sup>nd</sup>	Harvard Architecture, Mobile Devices Architecture (Android, Symbian and Windows Lite), Layered Approach Architecture		
15th	43 <sup>rd</sup>	Problem session		
	44 <sup>th</sup>	Problem session		
	45 <sup>th</sup>	Problem session		

(DR. RASHMI DAHRA)

PROFESSOR